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A Survey of Forward Gate Bias Stress Effect on the Noise Performance of Mesa Isolated GaN HEMTs

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Abstract

The study investigates degradation of gallium nitride (GaN) high-electron mobility transistor (HEMT) noise performance after both dc and RF stress with forward gate current. The results are used to facilitate optimization of the robustness of GaN low-noise amplifiers (LNAs). It is shown that forward biasing the gate of a GaN HEMT results in permanent degradation of noise performance and gate current leakage, without affecting S-parameters and drain current characteristics. The limit of safe operation of the 2 × 50 μm devices in this study is found to be between 10 and 20 mW dissipated in the gate diode for both dc and RF stress. We propose that degradation could be caused by excessive leakage through the mesa sidewalls at the edges of each gate finger. Circuit simulations may be used together with device robustness rating to optimize LNAs for maximum input power tolerance. Using a resistance in the gate biasing network of 10 kΩ, it is estimated that an LNA utilizing a 2 × 50 μm device could withstand input power levels up to 33 dBm without degradation in noise performance.

Keywords*: Semiconductor Device Noise, Semiconductor Device Reliability, Robustness, MODFETs, MODFET Amplifiers.*

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1. Introduction

Due to its combination of high power handling capability and low noise figure, the Gallium Nitride (GaN) High Electron Mobility Transistor (HEMT) has received much attention for its potential in highly rugged low noise amplifiers (LNAs). A High-electron-mobility transistor (HEMT), also known as heterostructure FET (HFET) or modulation-doped FET (MODFET), is a field-effect transistor incorporating a junction between two materials with different band gaps (i.e. a heterojunction) as the channel instead of a doped region (as is generally the case for MOSFET). A commonly used material combination is GaAs with AlGaAs, though there is wide variation, dependent on the application of the device. HEMT transistors are able to operate at

higher frequencies than ordinary transistors, up to millimeter wave frequencies. Destructive tests have shown that LNAs with GaN transistors survive input power levels more than one order of magnitude higher than a typical Gallium Arsenide (GaAs) LNA [1]. The use of GaN technology thus alleviates or eliminates the need of protection circuitry in receivers, potentially improving noise figure and decreasing complexity of the system. To validate that GaN is a reliable candidate technology for highly robust LNAs, it is important to study potential mechanisms of degradation that devices may experience during operation. In particular for LNA applications, it is important to study degradation affecting noise figure and gain.

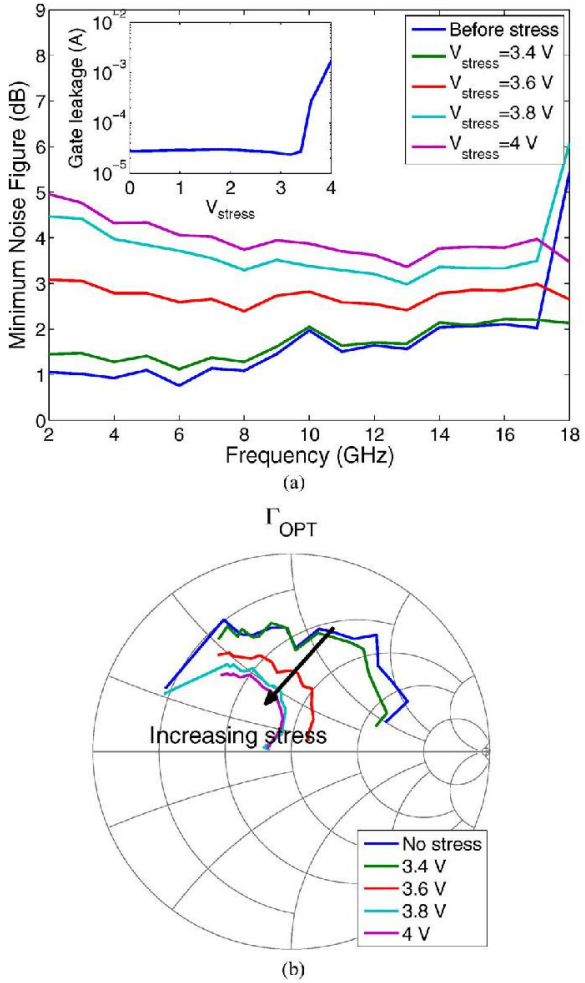

Fig. 1. Measured (a) minimum noise figure and (b) optimum source impedance after different stages of the stress test. The changes in noise parameters were accompanied by an increase in the reverse gate leakage, shown in the inset in (a).

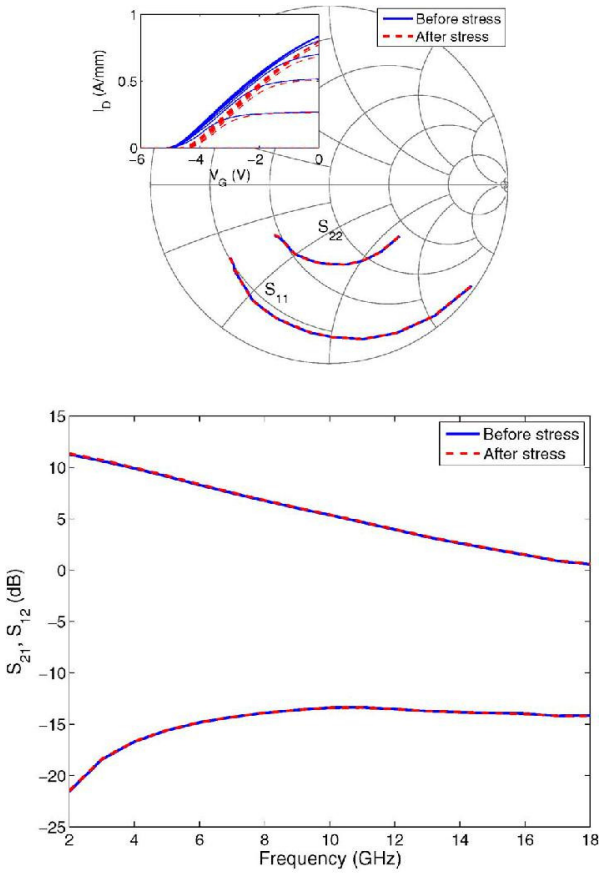

Fig. 2. Measured S-parameters and $I_D - V_G$ characteristics before and after stress.

Several studies have investigated different mechanisms causing performance degradation in GaN transistors. Stress with large gate-drain voltages is known to result in permanent decrease in maximum drain current and trans-conductance along with increase of drain resistance, gate leakage current, and gate lag phenomena [2]. This has been attributed to crystal deformations in

the gate–drain region, caused by high electric fields through the inverse piezoelectric effect [3]. Hot electrons are also believed to cause degradation when devices are subjected to simultaneous high currents and voltages [4]. Degradation due to forward gate current has been less studied. Large gate current may occur at high input power levels, which could be caused by jammers or other electronic warfare components. It was shown in the article of [5,6,7,8] that forward biasing the gate with large current causes a permanent increase of the reverse leakage current. Similar effects are seen after RF stressing an amplifier [1]. Although the degradation0020mechanism is not conclusively known, the authors of [5,6,7,8) all suggest degradation of the Schottky contact due to high temperature as the most likely cause of the increased gate current. In this work, degradation in GaN HEMTs after dc and RF forward gate current stress is further investigated, focusing on implications for system robustness and performance. We specifically address the case where the devices are isolated using an etched mesa, with the gate fingers extending outside the mesa and directly contacting the GaN channel through the mesa sidewall, giving rise to an additional conduction path for the gate current. The effect of this leakage path on the reverse leakage has been studied in [9], but the effects on device robustness have previously not been tested. Moreover, it is shown how degradation tests on device level can be used to analyze or optimize robustness of LNAs using circuit level simulations.

2. Effects of Gate Bias Stress on Noise Performance

S-and noise parameters of dc-stressed devices were measured to evaluate the effect of forward bias stress on noise performance. Measurements were performed on 0.25μm gate length AlGaN/GaN HEMTs fabricated in a Chalmers in-house MMIC process [9]. For the noise measurements, devices with 4×75μm gate periphery were used. The HEMTs were dc-stressed for 5 minutes by applying a constant positive dc voltage on the gate while keeping the drain and source terminals grounded. After each stress session the noise parameters between 2–18GHz at a low noise bias (10V and 50mA, corresponding to 20% of IDSS). This process was repeated for stress voltages stepped from 0V to 4V in 0.2V steps.

The stress resulted in changes in the transistor noise parameters, accompanied by an increase of reverse gate leakage (Fig.1). Specifically, the minimum noise figure increased from around 1.5dB to 4dB at 10GHz and the optimum source impedance shifted towards the center of the Smith chart, particularly for low frequencies. The drain current characteristics were largely unchanged apart from a 0.5V shift in the pinch-off voltage towards less negative values. Similar burn-in effects on the threshold voltage have previously been seen in other GaN HEMT processes [11] and do not explain the dramatic degradation in the noise performance, and the effects are not necessarily related. There are no significant differences between the S-parameters measured before and after stress for the same drain current and voltage (Fig.2). The explanation to the dramatic effects on $F_{\min}$ and Γ_{opt} despite the S-parameters being unchanged is instead the increase in gate leakage, which is known to result in degradation of noise performance due to the increased shot noise through the gate [12]. The reason for the increase in gate leakage is further studied in the following sections.

3. DC and RF Robustness Characterization

For successful design of highly robust LNAs, it is important to know which operating conditions the transistor can sustain without permanent damage. Therefore, more detailed stress tests were

conducted on several GaN HEMTs from the same wafer, in order to find the limiting factors of safe operation in terms of forward gate bias and RF input power rating.

A) *Setup & Procedure*

DC stress was performed on 2×50μm gate periphery devices in the same way as described in Section 2 and the dc *I–V* characteristics were measured after each stress session. The current was measured continuously during the stress. RF input power stress was also performed on a 2×50μm transistor in order to compare the degradation seen during constant dc forward bias to a more realistic case where the device is forward biased by the RF swing. The device was subjected to RF input power stress for five minutes at a typical LNA operation bias (V_{gs} = −4V and V_{ds} = 10V). A large signal network analyzer (LSNA) was used to measure the current and voltage waveforms at the input during stress. The RF input power was increased in steps from +17dBm to +27dBm. After each RF power stress level, the dc characteristics were measured. The RF frequency was chosen as low as possible with the available equipment (600MHz), to facilitate deem-bedding of the pads, the series resistance and the nonlinear gate capacitance.

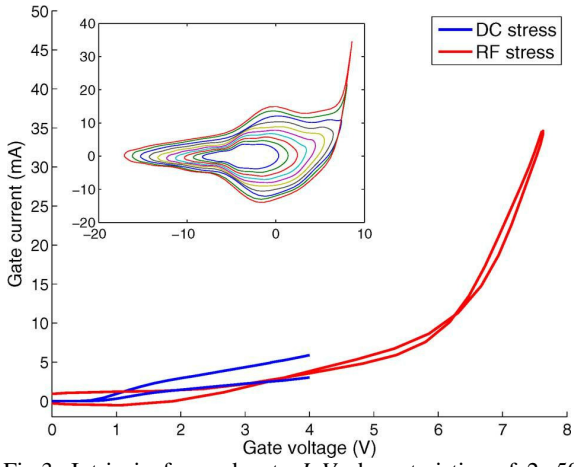

Fig.3. Intrinsic forward gate *I–V* characteristics of 2×50μm HEMT, during dc and RF stress. Two dc-stressed HEMTs and one RF-stressed with +27dBm available input power are shown. The intrinsic RF gate voltage is de-embedded from the measured extrinsic waveforms shown in the inset for different RF power levels. The available power levels for the different stress sessions were chosen so as to have a constant 1 V increase in voltage amplitude between each session ($P_{in,dBm}$ = 16.7, 18.6, 20.1, 21.4, 22.6, 23.6, 24.4, 25.3, 26.0, 26.7).

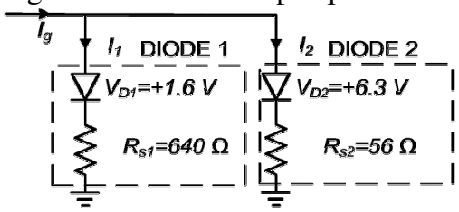

Fig. 4. Model of the gate diode of devices under test

B) Gate Diode Characterization

To understand what happens during stress, it is important to study the forward gate *I–V* characteristics of the devices under test. Fig. 3 shows the measured dc characteristics during dc stress and the intrinsic waveform during RF stress. The measured extrinsic waveforms from which the intrinsic curves were extracted are shown in the inset. Under dc conditions, forward conduction starts from around 0.8V forward biases and initially has a large series resistance, varying between 350Ω and 700Ω for different devices. The gate current (and the diode series resistance) does not scale with the gate periphery of the device. One dc-stressed device with a low series resistance and one with a high resistance are shown in Fig. 3.

The RF measurement is not directly comparable since there is also a voltage on the drain terminal, but the characteristics for low forward voltages is similar to the dc case with a high series resistance. However, the RF measurement also reveals that another diode turns on at ~5.5V, where the series resistance decreases to around 60Ω. This behavior cannot be seen under dc conditions since the devices suffer catastrophic failure before the second turn-on region is reached. Based on these observations, an equivalent circuit is extracted (Fig.4), which describes

the dc and RF forward characteristics of the gate (Fig.5). Leakage through the sidewalls of the mesa used for device isolation may be a physical explanation to this behavior, since it provides an additional Schottky diode directly to the GaN channel at the edges of each gate finger where the gate metal extends outside the mesa [9] (Fig.6). This diode is expected to turn on at lower forward voltages than the AlGaN Schottky diode, because of GaN's lower band gap. This, together with the observation that diode 1 (Fig.4) has a high series resistance which does not scale with gate periphery per finger, makes it probable that diode 1 is associated with the sidewall leakage, concentrated in a small area at the edges of each finger. The second turn-on of diode 2 starting around 5.5 V is then associated with the common gate diode. If the two diodes in Fig. 4 are physically separated, damage due to high gate current could be localized to one of them and both components should be considered separately when evaluating the robustness of the devices.

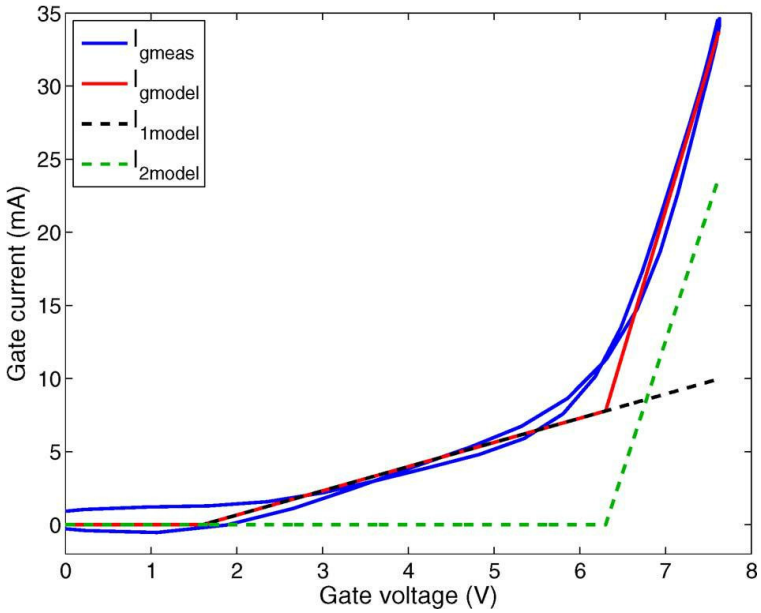

Fig.5. Forward *I–V* characteristics of the model in Fig. 4, compared to RF waveform measurement with parasitic de-embedded. The solid blue line shows the measured waveform after de-embedding and the solid red line the characteristics of the model in Fig. 4. The two dashed lines represent I_1 and I_2 in Fig. 4.

C) Effects on Reverse Gate Leakage

The dc stress resulted in permanent degradation of the gate current–voltage characteristics, with large increases of gate leakage both in the forward and reverse direction. Fig. 7(a) shows the $I_G - V_G$ characteristics for one device after different stages of the stress test. Degradation started at dc forward voltages higher than 2.8V, and another dramatic increase of gate leakage occurred at 3.8V. At dc forward bias, the devices were thus severely damaged before reaching the turn-on of diode 2 (Fig.4). It is thus likely that the main contribution of stress effect is caused by degradation in diode 1. For RF stress, devices experienced similar degradation (Fig.7(b)). The first noticeable effects on

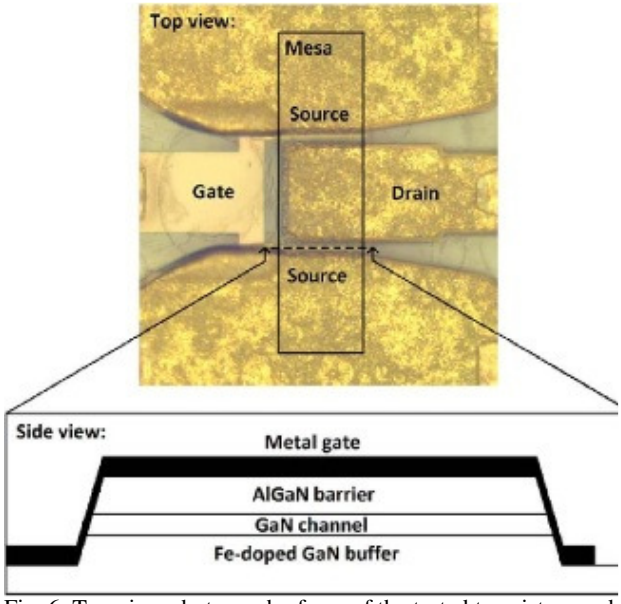

Fig. 6. Top view photograph of one of the tested transistors and a schematic cross-section view of the device along one of the gate fingers. The unit gate width is 50μm.

the $I_G - V_G$ characteristics occurred for an input power of 25.3dBm, corresponding to an intrinsic peak gate voltage and current of 10mA and 6V respectively. The dc component was 2mA and the gate power dissipation 10mW at this input power very severe degradation was seen after an input power of 26.7dBm corresponding to of 35mA peak current, 7V peak V_{gs}, 5.5mA dc current and 36mW power dissipation.

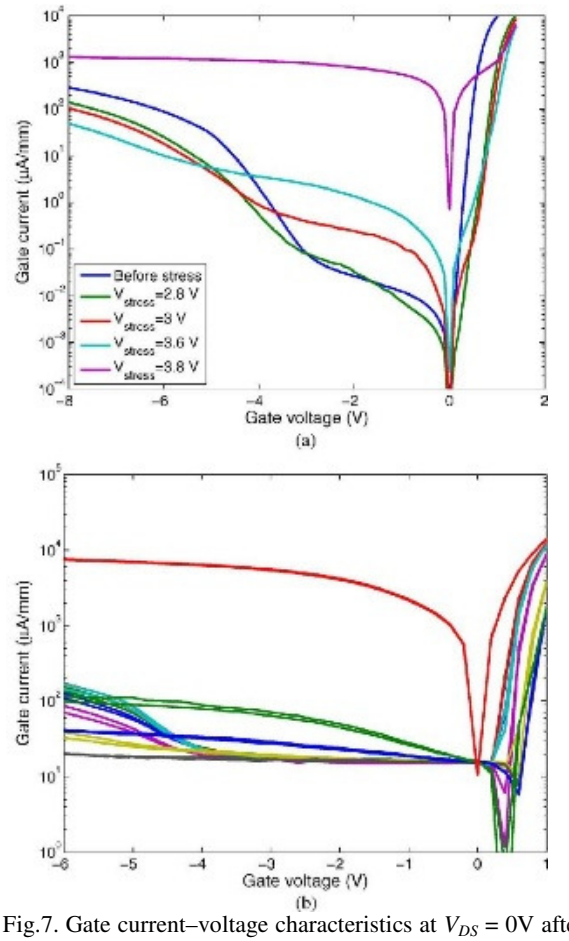

Fig.7. Gate current–voltage characteristics at V_{DS} = 0V after different stages of the (a) dc and (b) RF stress test. The dc forward bias is swept from 0 V to +4 V and the available RF input power is swept from +17dBm to +27dBm. The colors in (b) correspond to measurements after different stress sessions in Fig. 3.

Fig. 8 shows a comparison between degradation after dc and RF stress, displaying gate leakage for $V_{GS} = -4$V as a function of stress level, in terms of gate voltage, current and dissipated power in the gate. The two dc stressed devices, exhibiting different series resistance, start to degrade at a similar forward voltage, even though the corresponding gate current is significantly different. At a first glance this indicates an electric field induced degradation mechanism. In this case, the fact that the RF stressed device survived peak voltages up to 6V without notable degradation, whereas the dc stressed devices degraded below 4V points to a degradation mechanism slower than the length of the RF gate current pulses, which are in the nanosecond scale. However, the complete picture is more complicated and a current or dissipated power induced degradation mechanism cannot be excluded. The damage may be localized and the global current level does not necessarily reflect local current densities. For example, the variation in critical current and power dissipation between different devices may be due to variations in the not so well defined area of the mesa sidewall diode (diode 1).

When comparing the RF and dc case, it is important to note that local current density in diode 1 or 2 may be the cause of failure during RF stress whereas only diode 1 is conducting during dc forward bias, making the current highly localized to the mesa sidewalls. This could explain the large differences in power dissipation and dc current required to damage the devices between the dc and the RF case. In fig. 8(b) and (c) the contribution of diode 1 as extracted from the model is displayed separately. When only considering the current through diode 1, the large discrepancy between dc and RF stress disappears, and the diode degrades at similar current and power dissipation levels as during dc stress. If the degradation is power or current induced, this could be an indication that the current associated with mesa leakage, alone is responsible for degradation also during RF stress. In conclusion, based on these result it is not possible to isolate one main failure mechanism. Furthermore, a dual gate diode model is needed to enable accurate prediction

of the device characteristics in a circuit simulator.

4. Amplifier Robustness Analysis

In an LNA, it is common to protect the transistor from excessive forward conduction by using a large series resistance (typically in the kΩ range) in the gate bias network [13]. When dc current starts to flow, the voltage drop over the gate bias resistance causes the dc gate voltage to decrease, limiting the forward gate current. However, other studies have shown that large negative gate voltages are also harmful to devices and cause degradation [3,4,5]. The amplifier robustness is thus determined by the transistor's survivability to both forward and reverse bias stress, in interplay with its gate *I–V* characteristics, the bias resistance and the matching network. Evidently, there is a trade-off in choosing the series resistance to avoid both forward and reverse bias.

Based on the current, voltage and power dissipation levels presented above, we may define a region of safe operation. If the transistor's *I–V* characteristics and region of safe operation are known, harmonic balance simulations can be used to simulate the sustainable input power of an amplifier and optimize the bias resistance for maximum robustness. To demonstrate this, we use a simple model of an LNA input, using the model in Fig. 9 with a 2 × 50μm HEMT. The transistor is assumed to be matched to impedance close to 50Ω at the gate. In real LNAs, this value depends on frequency, device size and the matching networks, but the size is often chosen as to provide simple matching to 50Ω at the design frequency. Losses in the input matching network and parasitic resistances are not included in this model, so the robustness will likely be higher in real amplifiers.

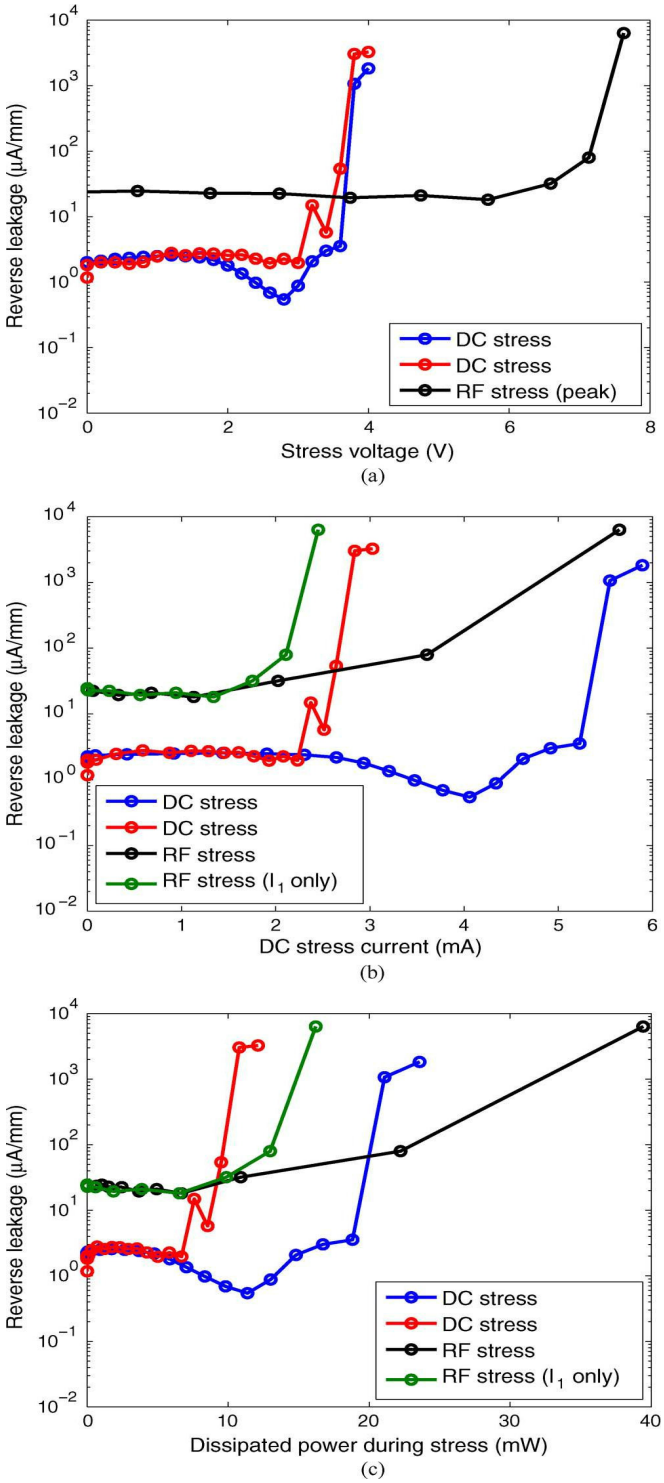

Fig.8. Comparison of degradation after dc stress and RF stress. The degradation of gate leakage at a gate bias of −4V is plotted as a function of forward voltage (a), forward gate current (b) and dissipated power in the gate (c). Two otherwise similar dc-stressed devices are shown, one with low series resistance below 5.5V and one with high resistance.

Assuming for example that power dissipation in the mesa sidewall diode is the main cause of failure during forward bias stress, we plot contours of the power dissipation in both diodes and gate voltage as functions of available input power and bias resistance (Fig. 10). According to the stress tests in this paper, the power dissipation in diode 1 should not exceed 7.5mW. A typical value of the critical drain–gate voltage for degradation is 30V [5], which mean that if the drain is biased at 10V, the gate voltage should not go below −20V. The maximum input power that can be sustained without running into any of these limits would then be approximately 33dBm, which is achieved with a resistance of 10kΩ. The power dissipation in diode 2 is then around 1mW, corresponding to 10mA/mm. Choosing the resistance too small is more detrimental to robustness than choosing it too large, since the current increases rapidly for decreasing resistance whereas the dc voltage drop increases more slowly when the resistance increases (Fig. 10).

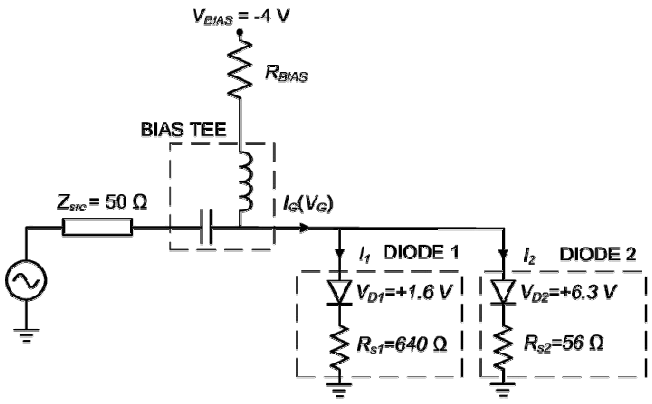

Fig. 9. Simplified model of the input of a low noise amplifier for analysis of gate current waveforms.

5. Discussion

The devices under test in this study have very different forward gate *I–V* characteristics compared to previous studies of degradation due to forward gate current, which have used devices with a more traditional diode behavior, turning into full conduction between 1V and 2V [5,6,7,8]. Whereas the effects on the devices from forward bias stress are similar in these studies and the dc voltages required to damage the devices in the same range, the devices in this study therefore suffered degradation at much lower gate current densities than in [5,6,7,8]. This is in line with the proposed leakage path through the mesa edge, since the current is concentrated to a very small area which could lead to localized damage.

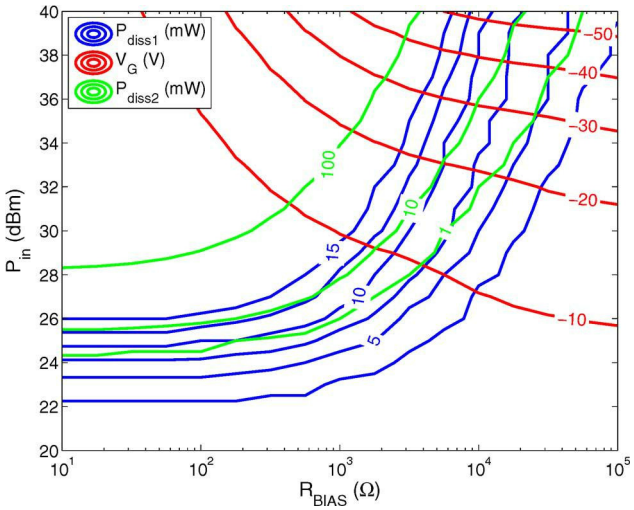

Fig.10. Simulated contours of dc voltage over and of power dissipation in the two diodes in Fig. 9, for different available input power and bias series resistance.

This has important effects on LNA robustness. Doing the analysis in Section 4 using the results from [7], where the devices withstood a gate current of 900mA/mm and voltage of 3.5V without severe degradation, would result in an optimal bias resistance of 30Ω • mm, giving a maximum input power of 43dBm for a 2 × 50μm device. Minimization of mesa leakage or use of other methods such as ion implantation, which can provide device isolation without the formation of a mesa where the GaN channel is in contact with the gate metal [14], could thus be essential for robust LNA design.

6. Conclusion

DC and RF stress tests have shown that devices subjected to forward gate bias stress degrade permanently, resulting in increased reverse gate leakage and impaired noise performance. More detailed analysis of the devices under test showed that the devices behave like two parallel gate diodes under forward bias. The high resistance diode that dominates for low forward bias voltages is proposed to be associated with mesa sidewall leakage and seems to cause degradation during both dc and RF stress in this study. Circuit simulations have been used to estimate that a 2 × 50μm transistor used in an LNA survives 33dBm input power to the gate if a 10kΩ resistor is used in the gate bias network, given the damage levels indicated by stress tests. Device design for optimizing LNA robustness should focus on gates with minimized mesa leakage. The increase in noise figure resulting from forward bias stress could significantly degrade the sensitivity of a GaN receiver. The stress effects can most easily be followed by monitoring the gate current or the noise figure in the system, as the increase in noise figure is noticeable at stress levels far below the levels required to affect S-parameters and output characteristics.

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